IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Matthew B. Haycock et al.

Title:

BIDIRECTIONAL PORT WITH CLOCK CHANNEL USED FOR SYNCHRONIZATION

Docket No.:

P.O. Box 1450

884.509US2

Filed:

October 21, 2003

Examiner:

Daniel Chang

Commissioner for Patents

Alexandria, VA 22313-1450

Serial No.: 10/690235

Due Date: May 24, 2004

Group Art Unit: 2819

We are transmitting herewith the following attached items (as indicated with an "X"):

- \underline{X} A return postcard.
- X A Response Under 37 C.F.R. 1.111 (5 Pages).
- X A Communication Concerning Related Applications (2pgs).
- X A Supplemental Information Disclosure Statement (2 pgs.), Form 1449 (1 pg.), and copies of 6 cited documents.
- X Terminal Disclaimer (3 pgs.).
- X Authorization to charge Deposit Account in the amount of \$110 for Terminal Disclaimer Fee and in the amount of \$180.00 to cover the fee for consideration of Information Disclosure Statement under 97(c)

If not provided for in a separate paper filed herewith, Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

Customer Number 21186

Atty: John M. Dahl Reg. No. 44,639

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Azne M. Richards

Name

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

(GENERAL)

4

S/N 10/690235 PATENT

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Applicant: Matthew B. Haycock et al.

Examiner: Daniel Chang

Serial No.:

10/690235

Group Art Unit: 2819

Filed:

October 21, 2003

Docket: 884.509US2

Title:

BIDIRECTIONAL PORT WITH CLOCK CHANNEL USED FOR

SYNCHRONIZATION

COMMUNICATION CONCERNING RELATED APPLICATION(S)

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

Serial/Patent No. 09/644463	Filing Date A August 23, 2000	sttorney Docket 884.303US1	Title SIMULTANEOUS BIDIRECTIONAL PORT WITH SYNCHRONIZATION CIRCUIT TO SYNCHRONIZE THE PORT WITH ANOTHER PORT
09/659499 6424175	September 11, 2000	884.307US1	BIASED CONTROL LOOP CIRCUIT FOR SETTING IMPEDANCE OF OUTPUT DRIVER
09/694901 6445170	October 24, 2000	884.333US1	CURRENT SOURCE WITH INTERNAL VARIABLE RESISTANCE AND CONTROL LOOP FOR REDUCED PROCESS SENSITIVITY
09/824370 6448811	April 2, 2001	884.403US1	INTEGRATED CIRCUIT CURRENT REFERENCE
09/835600 6507225	April 16, 2001	884.450US1	CURRENT MODE DRIVER WITH VARIABLE EQUALIZATION
09/951909 6529037	September 13, 2001	884.508US1	VOLTAGE MODE BIDIRECTIONAL PORT WITH DATA CHANNEL USED FOR SYNCHRONIZATION
09/894865	June 28, 2001	884.509US1	BIDIRECTIONAL PORT WITH CLOCK CHANNEL USED FOR SYNCHRONIZATION

COMMUNICATION CONCERNING RELATED APPLICATIONS

Serial Number: 10/690235 Filing Date: October 21, 2003

Title: BIDIRECTIONAL PORT WITH CLOCK CHANNEL USED FOR SYNCHRONIZATION

Page 2 Dkt: 884.509US2

09/972327 6597198 October 5, 2001

884.527US1

CURRENT MODE BIDIRECTIONAL PORT WITH DATA CHANNEL USED FOR SYNCHRONIZATION

Respectfully submitted,

MATTHEW B. HAYCOCK ET AL.

By Applicants' Representatives,

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Anne M. Richards

Name

Signature